What is claimed is:

1. A fractional-N frequency synthesizer, comprising:

a phase detector for detecting a phase difference between a reference signal and a feedback signal;

a voltage controlled oscillator for receiving a phase difference control signal based on the detected phase difference, and for oscillating a signal with a frequency based on the detected phase difference;

a divider for selecting a value from at least three integers according to a predetermined selection signal, for dividing the frequency of the oscillated signal output from the voltage controlled oscillator by the selected value, and for outputting a divided signal as a feedback signal to the phase detector; and

a sigma-delta modulator for adding a predetermined input value to an internal feedback value, for successively accumulating added values, for quantizing an accumulated value to at least three levels, and for converting a quantized value into the predetermined selection signal.

2. The fractional-N frequency synthesizer of claim 1, wherein the sigma-delta modulator comprises:

a plurality of operation units for adding the predetermined input value to the internal feedback value and for successively accumulating the added values;

a quantizer for quantizing the accumulated value output from a last one of the plurality of operation units to a plurality of bits and for outputting the quantized value as the predetermined selection signal to the divider; and

a plurality of multipliers for outputting feedback coefficients as internal feedback values to each of the plurality of operation units, wherein the feedback coefficients are determined according to a quantized level corresponding to the plurality of bits.

3. The fractional-N frequency synthesizer of claim 2, wherein the feedback coefficients are symmetrical values spaced at equal intervals around a middle level of the at least three levels.

4. The fractional-N frequency synthesizer of claim 3, wherein the feedback coefficients are converted into bit streams with binary values.

5. The fractional-N frequency synthesizer of claim 4, further comprising a control signal generator for receiving a plurality of bit values output from the quantizer and for outputting a minimum number of control signals depending on symmetrical values of the bit streams.

6. The fractional-N frequency synthesizer of claim 5, wherein the control signal generator comprises:

a gray coder for converting the plurality of bit values into a gray code;

a plurality of control signal generating units for receiving the gray code and for outputting the control signals; and

a plurality of inverters for inverting outputs of the plurality of control signal generating units.

7. The fractional-N frequency synthesizer of claim 5, wherein the multipliers include connections for outputting the bit streams from the control signals of the control signal generator directly to the plurality of operation units.

8. The fractional-N frequency synthesizer of claim 6, wherein the multipliers include connections for outputting the bit streams from the control signals of the control signal generator directly to the plurality of operation units.

9. A sigma-delta modulator comprising:

a plurality of operation units for adding input values to internal feedback values and for successively accumulating the added values up to a fourth order;

a quantizer for quantizing an accumulated value output from a last one of the plurality of operation units into a plurality of bits; and

a plurality of multipliers for outputting feedback coefficients as internal feedback values to each of the plurality of operation units, wherein the feedback coefficients are determined according to a quantized level corresponding to the plurality of bits.

10. The sigma-delta modulator of claim 9, wherein the feedback coefficients are symmetrical values spaced at equal intervals around a middle level of a plurality of levels output from the quantizer.

11. The sigma-delta modulator of claim 10, wherein the feedback coefficients are converted into bit streams with binary values.

12. The sigma-delta modulator of claim 11, further comprising a control signal generator for receiving a plurality of bit values output from the quantizer and for outputting a minimum number of control signals depending on symmetrical values of the bit streams.

13. The sigma-delta modulator of claim 12, wherein the control signal generator comprises:

a gray coder for converting the plurality of bit values into a gray code;

a plurality of control signal generating units for receiving the gray code and for outputting the control signals; and

a plurality of inverters for inverting outputs of the control signal generating units.

14. The sigma-delta modulator of claim 12, wherein the multipliers include connections for outputting the bit streams from the control signals of the control signal generator directly to the plurality of operation units.

15. The sigma-delta modulator of claim 13, wherein the multipliers include connections for outputting the bit streams from the control signalsof the control signal generator directly to the plurality of operation units.

16. A frequency synthesizer, comprising:

a phase detector for detecting a phase difference between a reference signal and a feedback signal;

a voltage controlled oscillator for receiving a phase difference control signal based on the detected phase difference, and for outputting a signal with a frequency based on the detected phase difference;

a divider for selecting a value from a plurality of integers according to a predetermined selection signal, for dividing the frequency of the signal output from the voltage controlled oscillator by the selected value, and for outputting a divided signal as a feedback signal to the phase detector; and

a modulator for adding a predetermined input value to an internal feedback value, for successively accumulating added values, for quantizing an accumulated value to a plurality of levels, and for converting a quantized value into the predetermined selection signal.

17. The frequency synthesizer of claim 16, wherein the modulator comprises:

a plurality of operation units for adding the predetermined input value to the internal feedback value and for successively accumulating the added values;

a quantizer for quantizing the accumulated value output from a last one of the plurality of operation units to a plurality of bits and for outputting the quantized value as the predetermined selection signal to the divider; and

a plurality of multipliers for outputting feedback coefficients as internal feedback values to each of the plurality of operation units, wherein the feedback coefficients are determined according to a quantized level corresponding to the plurality of bits.

18. The frequency synthesizer of claim 17, wherein the feedback coefficients are symmetrical values spaced at equal intervals around a middle level of the plurality of levels.